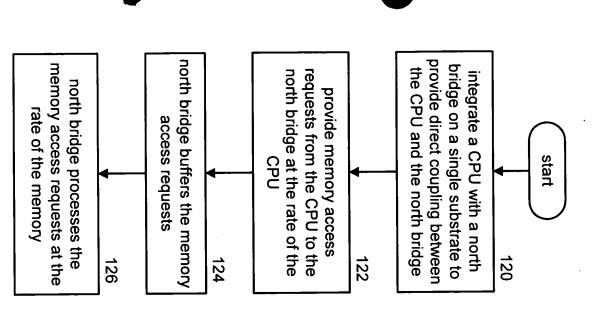


FIG. 3

100



memory access requests at the north bridge buffers the memory south bridge to the north bridge requests from the CPU and the bridge and a south bridge on a integrate a CPU with a north north bridge processes the provide memory access at the rate of the CPU rate of the memory access requests single substrate start 130 136 134 132

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FIG. 5

FIG. 6